REMARKS

Claims 1-22 are pending. Applicant has amended claim 7, 15, and 20 to clarify the subject matter of the invention.

Applicant's technology is directed to a technique for sectioning memory so that a subdivision of a word can be selectively enabled or disabled. For example, a memory bank may have a word length of 64 bits with two sections of 32 bits each. Each section thus represents a 32-bit subdivision of the word. When both sections are enabled, then an access to a memory location will access a 64-bit word. In contrast, when only one section is enabled, then that same access would only access a 32-bit word. A computer system that needs only 32-bit words can configure the memory bank so that one section is disabled. When a section is disabled, the "row enable lines" (also referred to as "wordlines") for that section cannot enable the rows of that section. Thus, when an address is decoded to a row, that row for only those enabled sections is enabled. As a result, when the memory bank is accessed, power consumption is reduced since the row enable line to only the enabled sections is enabled.

The Examiner has rejected claims 1-22 as being unpatentable based on the references as follows:

Claims	Statute	Reference
15, 20	35 U.S.C. § 102(b)	Amitai
16-19, 21-22	35 U.S.C. § 103(a)	Amitai, Getzinger
1-5, 7-13	35 U.S.C. § 103(a)	Amitai, Leung
6, 14	35 U.S.C. § 103(a)	Amitai, Leung, Getzinger

Applicant respectfully traverses these rejections.

The Examiner had previously rejected claims 1-14 based on Leung. Because Leung does not "teach each section of the bank representing a subdivision of a word of memory," the Examiner relies on Amitai to cure this deficiency. In particular, the Examiner

points to Amatai where it describes that "two CAS output signals can be selectively connected to a different 8-bit section or byte of the memory bank." (Amatai, 3:18-20.) As shown in Figure 5, the CAS0 and CAS1 ("column address strobe") lines are connected to a different 8-bit section of the DRAMs to enable byte 0 or byte 1, respectively, and the RAS0-3 ("row address strobe") lines are each connected to one of the DRAMs. Although not shown in Figure 5, the address lines are also connected to the DRAMs to select the appropriate memory address within the DRAMs. (See, Figure 7 address lines Q8-Q0.) As a result, when the CAS and RAS lines are strobed, the address is latched to the memory banks so that it can be decoded and the appropriate byte accessed.

Amatai, however, neither teaches nor suggests anything related to a "row enable line" (or "wordline"). An address is decoded into one of many row enable lines. For example, if the address is eight bits, then it is decoded into one of 256 row enable lines that each represents a word of memory. A row enable line enables the row representing the word of memory that is being accessed. Applicant's technology disables a section of a multi-section memory bank so that the row enable lines input to that disabled section are not enabled by the address decoding.

Amatai describes that the addresses are strobed, but does not describe how the addresses are decoded and how the row enable lines are enabled. The decoding of addresses and the row enable lines would be internal to the DRAM memory banks 20a-20d of Amatai, which are shown only in block form. Thus, Amatai is silent as to how row enable lines are handled internally within a DRAM memory bank.

Each of the claims recites that row enable lines for a section are enabled only when the section is enabled. Claims 1-6 recite "for each row of each section, row enabler logic that enables the row enable line for that row of that section only when the section enable line for that section is enabled." Claims 7-22 recite "row enable lines to a section are only enabled when the subdivision of the word represented by the section is accessed," or similar language.

Since none of the relied-upon references teaches or suggests that row enable lines for sections can be disabled on a section-by-section basis, applicant respectfully submits that the claims are neither anticipated by or obvious in view of the relied-upon references.

Based on the above amendments and remarks, applicant respectfully requests reconsideration of this application and its early allowance. If the Examiner has any questions or believes a telephone conference would expedite prosecution of this application, the Examiner is encouraged to call the undersigned at (206) 359-8548.

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Respectfully submitted,

By _____

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